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Subclass	ISSUE CLASSIFICATION
Class	

PATENT NUMBER

U.S. UTILITY Patent Application

O.I.P.E.	PATENT DATE
SCANNED AC 12 Q.A. VR	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/850228	F	~~716~~ 713	503	~~2184~~ 2182 2116	Lee PATEL

APPLICANTS: Satoru Kishimoto

TITLE: Placement and routing method for clock distribution circuit, clock distribution circuit manufacturing method, semiconductor device manufacturing method, clock distribution circuit and semiconductor device

PTO-2040 12/99

ISSUING CLASSIFICATION

ORIGINAL CLASS	ORIGINAL SUBCLASS	CROSS REFERENCE(S) CLASS	CROSS REFERENCE(S) SUBCLASS (ONE SUBCLASS PER BLOCK)

INTERNATIONAL CLASSIFICATION

☐ Continued on Issue Slip Inside File Jacket

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☐ The term of this patent subsequent to _____ (date) has been disclaimed.

☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____

☐ The terminal ___ months of this patent have been disclaimed.

DRAWINGS			CLAIMS ALLOWED	
Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.

_____ (Assistant Examiner) _____ (Date)

_____ (Primary Examiner) _____ (Date)

_____ (Legal Instruments Examiner) _____ (Date)

NOTICE OF ALLOWANCE MAILED

ISSUE FEE

Amount Due	Date Paid

ISSUE BATCH NUMBER

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